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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,596	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-9, 11-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 21, 2004 has been entered.

Response to Amendment

2. This Office Action is in response to the amendment filed on September 21, 2004.

Specification

3. The disclosure is objected to because of the following informalities:

Page 5 lines 3-4, "the interconnect 265 may include 8 differential pairs, 9 pairs for data, and 9 pairs for address and command." should be -- the interconnect 265 may include 18 differential pairs, 9 pairs for data, and 9 pairs for address and command.--

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to

> which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 3-4, 5-9 and 11-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 1 and 9, the limitation "an off-chip memory module" neither clearly disclosed in the drawing nor described in the specification. If Applicant believe it does disclosed in at the time the application was filed, please point it out to the examiner with the detail page and line numbers in the response.

Regarding claims 5 and 9, the limitation "a data cache including an eviction buffer" neither clearly disclosed in the drawing nor described in the specification. If Applicant believe it does disclosed in at the time the application was filed, please point it out to the examiner with the detail page and line numbers in the response.

Regarding claims 3-4, 6-8 and 11-12 are also rejected because of depending on claims 1, 5 and 9 respectively, containing the same deficiency.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3, the term "a second memory module memory device" is indefinite, because it is unclear whether is a second memory module or a second memory device.

The following are rejections are applied from what is best understood of the claim(s) in view of the 35 U.S.C. 112 First paragraph problems listed above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3-9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Saulsbury et al. (US PAT. 6,128,702).

Regarding claim 1, Stracovsky discloses a memory controller, i.e., universal controller (104, figure 1B), comprising an array of tag address storage location, i.e., resource tag (114, figure 1B), and a command sequencer and serializer unit, i.e. command sequencer (116, figure 1B), coupled to the array of tag address storage locations further determent the resources state of and location of the requested data stored in shared memory (108, figure 1B) and (col. 7 line 24

through col. 8 line 2 and col. 10 line 46 through col. 11 line 15), the command sequencer and serializer unit to control a data in an off-chip memory module, i.e., shared memory (108, figure 1B) via the memory command bus (220, figure 1B), command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the memory module (col. 6 lines 21-49, col. 11 line 22 through col. 12 line 19 and col. 13 lines 8-47). Stracovsky differs from the claimed invention in not specifically teaches a data cache and an eviction buffer located on at least one memory device of an off-chip memory module, the memory controller coupled to the memory module via a memory bus, the command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the data cache, the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to the eviction buffer located on the memory device. However, Saulsbury teaches the computer system (100, figure 1) comprising a memory controller, i.e., CPU (102, figure 1) and a memory module, i.e., system memory (103, figure 1) wherein the memory module comprising at least one memory device, i.e., victim data cache (106, figure 1), memory block (104, figure 1), wherein an eviction buffer, i.e., victim data cache line storage (160, figure 7) located on the memory device in an off-chip memory module, and a data cache, i.e., primary data cache (122, figure 1), in addition, Saulsbury teaches the memory controller is able to accessing the data from the data cache via the primary data cache bank logic (150, figure 2) which the memory accessing operation comprising a command to cause a previous line of data, i.e., victim data cache line, to be evicted out of the data cache an eviction buffer located on the memory device (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66). Therefore, it would have been obvious to a person of ordinary skill in

the art at the time the invention was made to modify the computer system Stracovsky in having a data cache located on each of memory bank and the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module, as per teaching of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation, because it greatly reduces the cache miss rate over conventional data caches that store data cache lines that are less than full-width.

Regarding claim 3, Saulsbury discloses the command sequencer and serializer to deliver a write-back command to the data cache associated with the memory module, the write back command to cause the previous line of data stored in the eviction buffer to be written out to a second memory module memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 4, Saulsbury discloses the write-back command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 5, Stracovsky discloses a memory module, i.e., shared memory (108, figure 1B) comprising at least one memory device (device type 1 – device type N, figure 1C), and a memory controller, i.e., universal controller (104, figure 1B) coupled to the shared memory via the memory bus (220, figure 1B), and the memory controller further generating the requested data and command from the processor (102, figure 1B) to the memory device (col. 6 lines 21-49, col. 11 line 22 through col. 12 line 19 and col. 13 lines 8-47), the memory controller including an array of tag address storage location, i.e., resource tag (114, figure 4) and (col. 7 line 24 through col. 8 line 2 and col. 10 line 46 through col. 11 line 15). Stracovsky differs from the claimed

invention in not specifically teaches a data cache coupled to the memory device, the memory controller to write a current line of data to the data cache, the memory controller to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory modules. However, Saulsbury teaches the computer system (100, figure 1) comprising a memory controller, i.e., CPU (102, figure 1) and a memory module, i.e., system memory (103, figure 1) wherein the memory module comprising at least one memory device, i.e., victim data cache (106, figure 1), memory block (104, figure 1), wherein an eviction buffer, i.e., victim data cache line storage (160, figure 7) located on the memory device in an off-chip memory module, and a data cache, i.e., primary data cache (122, figure 1), in addition, Saulsbury teaches the memory controller is able to accessing the data from the data cache via the primary data cache bank logic (150, figure 2) which the memory accessing operation comprising a command to cause a previous line of data, i.e., victim data cache line, to be evicted out of the data cache an eviction buffer located on the memory device (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system Stracovsky in having a data cache located on each of memory bank and the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module, as per teaching of Saulsbury, because it greatly reduces the cache miss rate over conventional data caches that store data cache lines that are less than full-width.

Regarding claim 6, Saulsbury discloses the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Regarding claim 7, Saulsbury discloses the memory module to receive a write-back command that generated by the memory controller, the write-back command to cause the previous line of data to be written out of the eviction buffer to the memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 8, Saulsbury discloses the write-back command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 9, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller, i.e. universal controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B), the memory controller including an array of tag address storage location, i.e., resource tags (114, figure 1B) and a command sequencer and serializer unit, i.e., command sequencer (116, figure 1B) coupled to the array of tag to determent the resources state of and location of the requested data stored in shared memory (108, figure 1B) and (col. 7 line 24 through col. 8 line 2 and col. 10 line 46 through col. 11 line 15), and an off-chip memory module (108, figure 1B) coupled to the memory controller via a memory bus (220, figure 1B), the memory module including at least one memory device (device type 1 – device type N, figure 1C). Stracovsky differs from the claimed invention in not specifically teaches a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a

current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer. However, Saulsbury teaches such as rejected as the same in claims 1 and 5. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Stracovsky in having a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer, as per teaching by the computer system of Saulsbury, because it greatly reduces the cache miss rate over conventional data caches that store data cache lines that are less than full-width.

Regarding claim 11, Saulsbury discloses the memory controller to deliver a write-back command to the data cache, the write-back command to cause the previous line to written out of the eviction buffer to the memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 12, Saulsbury discloses the write-back command including way information and back address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Response to Arguments

10. Applicant's arguments filed September 21, 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, In this case, Stracovsky and Saulsbury are combinable because they are in the same field of endeavor, i.e., a data processing system having a multiple memory banks device. In addition, Stracovsky teaches a backbone structure of the data processing system including a memory controller, i.e., universal controller, which comprising a tag, i.e., resource tags, and a command sequencer, i.e., command sequencer and serializer unit, and a system memory comprising a plurality of devices (figures 1B-1D). Although Stracovsky fails to specifically teach the system memory comprising a data cache, and an eviction buffer located on at least one memory device, and a previous cache line of data to be evicted out of the data cache to the eviction buffer located on the memory device, such limitation is taught by Saulsbury (see rejection above). Note while Stracovsky also teaches memory device comprising a plurality of blocks and controlled by the CPU, i.e., memory controller, (figure 1). Thus, Stracovsky and Saulsbury and combinable, and the motivation of Stracovsky and Saulsbury is to reduces the cache miss rate over conventional data caches that store data cache lines that are less than full-width (see Saulsbury col. 15 lines 30-33).

In response to the newly amended claim 5, the newly amended limitation "a data cache including an eviction buffer" is inconsistent with the limitation "the memory controller to cause a

previous line of data to be evicted out of the data cache to the eviction buffer located on the memory device", because how would the previous line of data to be evicted out of the data cache if an eviction buffer is included in the data cache.

In response to the to Applicant's argument that neither Stracovsky nor Saulsbury teaches the memory module is an off-chip memory module, examiner recognizes that Applicant fails to clearly disclosure the newly amended limitation in the specification or drawings (see rejected under 35 U.S.C. 112 First paragraph above). In addition, the specification of Applicant's invention only disclosures the computer system includes a processor, memory controller, and a system memory coupled to the memory controller via a memory bus as defined in figure 1 and (Pp [0014]-[0016]). Furthermore, the claims are interpreted as the broadest reasonable interpretation, since Stracovsky teaches system comprising requesting device, a universal device controller, and a shared resource, which connected by system bus (figure 1B), thus, Stracovsky is enough to rejected based on the broadest claim language.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

November 3, 2004

MATTHEW ANDERSON
PRIMARY EXAMINER
GROUP 2100